Amendments to the Specification:

On page 6, please amend the paragraph beginning at line 25 as follows:

"The equalizer (110) includes an input terminal (IN), an output terminal (OUT), and a control input terminal (CTL). The equalizer receives a data signal (DATAIN) through the input terminal (IN). The equalizer produces an output signal (EQOUT, 112) through the output terminal (OUT). The equalizer is controlled by a control signal (EQCTL, 162) that is received through the control input terminal (CTL). The shape of the output signal (EQOUT, 112) corresponds to a shaped version of the data signal (DATAIN), where the waveform shaping is controlled by the control signal (EQCTL, 162)."

On page 8, please amend the paragraph beginning at line 3 as follows:

"The digital control logic (160) includes two input terminals (IN1, IN2) and two output terminals (OUT1, OUT2). One of the input terminals (IN1) receives the output signal (DLYOUT, 132) or signals from the timing delay (130). The other of the input terminals (IN2) receives the output signal (CPOUT, 152) from the comparator (150). The digital control logic produces control signals in response to the input signals (DLYOUT, CPOUT). One of the control signals (EQCTL, 162) is coupled through the one of the output terminals (OUT1). The other of the control signals (PDCTL, 164) is coupled through the other output terminal (OUT2). The EQCTL signal is used to adjust the equalization level in the equalizer (110). The PDCTL signal is used to adjust the peak detector output level in the peak detector (140)."

On page 14, please amend the paragraph beginning at line 21 as follows:

"In accordance with the present invention, an exemplary digital control logic block is shown in FIGURE 8. The digital control logic (800) includes a sampling logic block (810), an equalizer control block (820) and an amplitude control block (830). The sampling logic block (810) receives timings signals (802) and comp_out (804) from the timing delay and comparator blocks (see FIGURES 1 and 2). For example, in one embodiment of the present invention the timing signals (802) correspond to T2_SIG and T3_SIG and the COMP_OUT signals (804) correspond to CPOUT (252) as shown in FIGURE 2. The sampling control generates sample

data (812) in response to the input signals. The equalizer control block (820) receives the sample data (812) and produces an equalizer control signal (822, EQCTL). The amplitude control block (830) receives the sample data (812) and produces an amplitude control signal (AMPCTL, 832). A reset signal (806) is also received by the sampling logic (810), the equalizer control (820), and the amplitude control (830) blocks. The reset signal (806) may be used to periodically reset the digital control logic block such that the ~~outputs~~ output signals are in a predictable state. In one example, the reset signal corresponds to a power-on reset signal that initializes all logic in the system. In light of the above described features in the present invention, it is understood and appreciated that blocks 810-830 may be combined or separated into one or more, and additional blocks may be included in the digital control logic."

On page 18, please amend the paragraph beginning on line 26 as follows:

"An example averaging algorithm control logic for equalization control is shown in FIGURE 12. The equalizer control (1200) includes a decoder logic block (1210), a state logic block (1220), a counter block (1230), and an equalizer setting block (1240). The decoder logic block (1210) receives the sample data points (T1_SP1, T3_SP1) from the sampling logic block previously discussed, and generates two signals (OVERSHOOT, UNDERSHOOT). One of the timing signals (T3_SIG) from the timing delay block previously discussed is used as a clock signal for the state logic (1220). The timing signal (T3_SIG) may also be used as a clock signal for the counter (1230) and equalizer setting (1240) blocks. The state logic (1220) generates four output signals (RST, EN, UP and DWN) in response to five signals (OVERSHOOT, UNDERSHOOT, T3_SIG, CNT and RESET) that it receives. The counter block (1230) generates a count signal (CNT) in response to the RST, EN, and T3_SIG signals. The equalizer setting block (1240) produces the EQCTL signal in response to the UP, DWN, ~~and~~ T3_SIG, and RESET signals."

On page 20, please amend the paragraph beginning at line 18 as follows:

"An example averaging algorithm control logic for amplitude control is shown in FIGURE 13. The amplitude control (1300) includes a decoder logic block (1310), a state logic block (1320), a counter block (1330), and an amplitude setting block (1340). The decoder logic block (1310) receives the sample data points (T1_SP1, T3_SP1) from the sampling logic block previously discussed, and generates two signals (OVERAMPLITUDE, UNDERAMPLITUDE). One of the timing signals (T3_SIG) from the timing delay block previously discussed is used as a clock signal for the state logic (1320). The timing signal (T3_SIG) may also be used as a clock signal for the counter (1330) and amplitude setting (1340) blocks. The state logic (1320) generates four output signals (RST, EN, UP and DWN) in response to five signals (OVERAMPLITUDE, UNDERAMPLITUDE, T3_SIG, CNT and RESET) that it receives. The counter block (1330) generates a count signal (CNT) in response to the RST, EN, and T3_SIG signals. The amplitude setting block (1340) produces the AMPCTL signal in response to the UP, DWN ~~and~~, T3_SIG, and RESET signals."